09656274 120500

Fig. 1

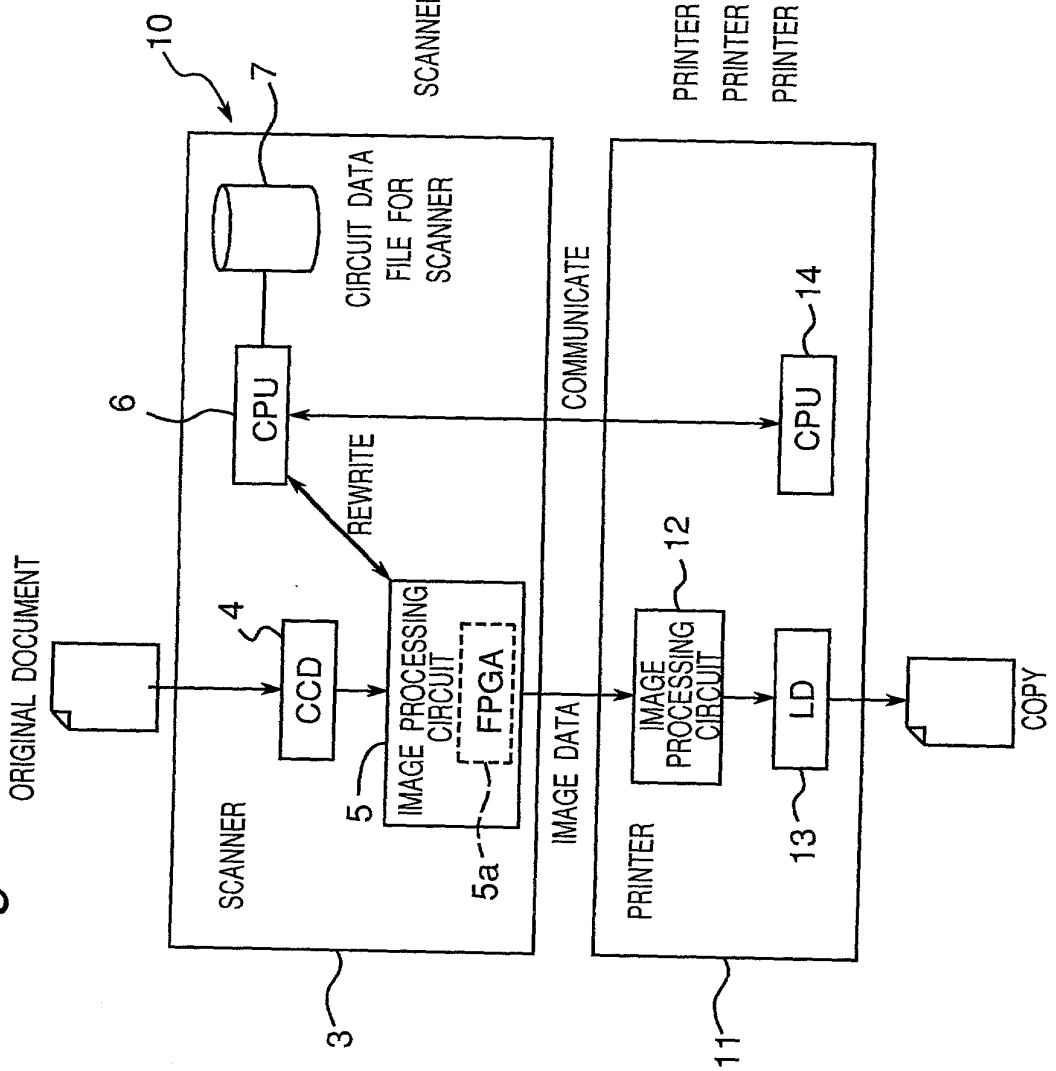
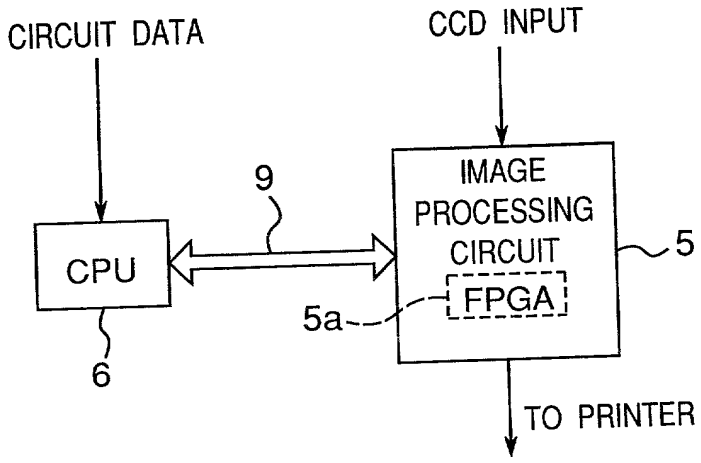


Fig.2


CIRCUIT DATA
CCD INPUT
9
IMAGE
PROCESSING
CIRCUIT
5
CPU
FPGA
5a
6
TO PRINTER

0070251 "EP99926"

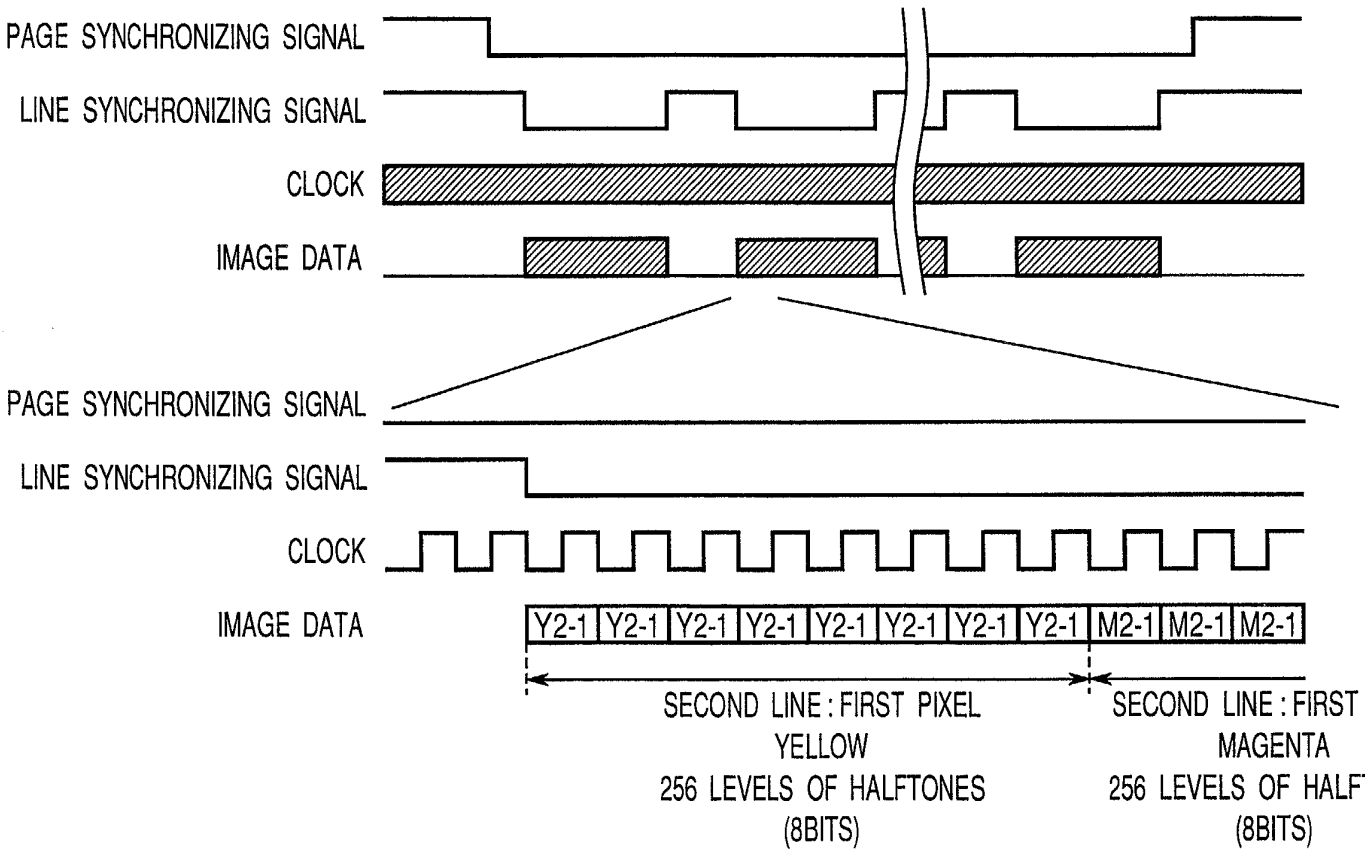


Fig.3A

Fig.3B

0070054 "EP 0 398 269 A2"

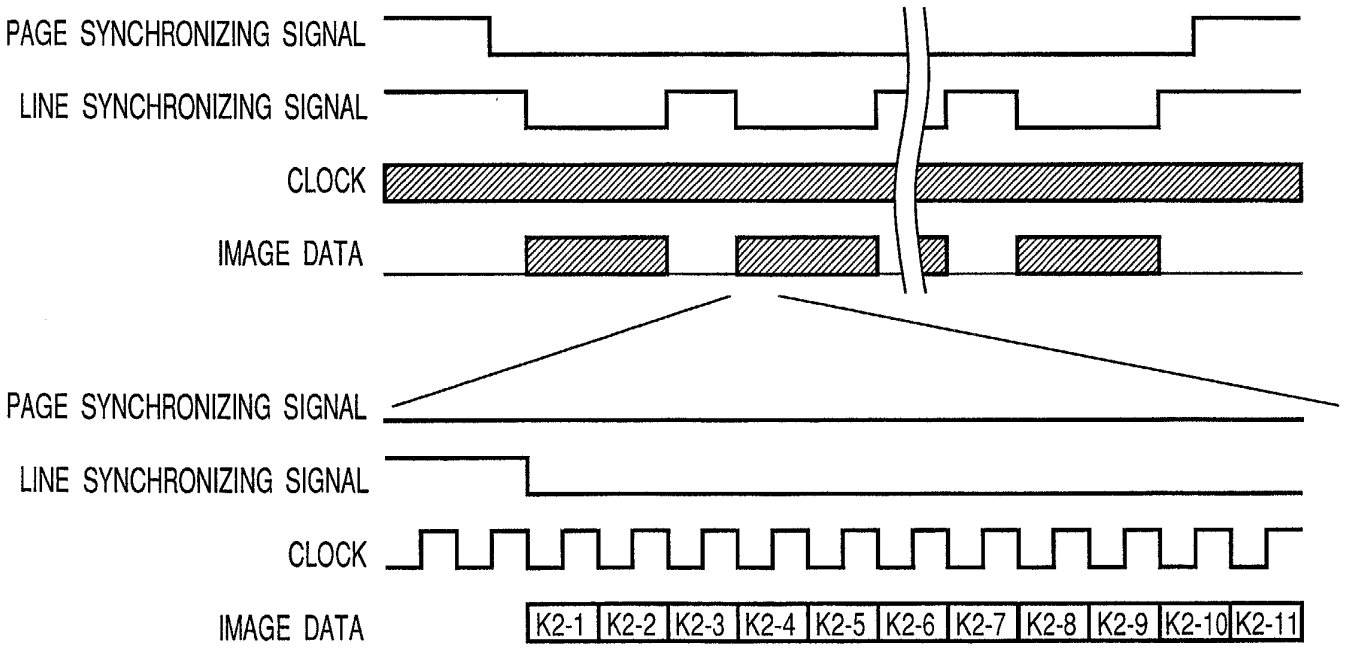


Fig.4A

Fig.4B

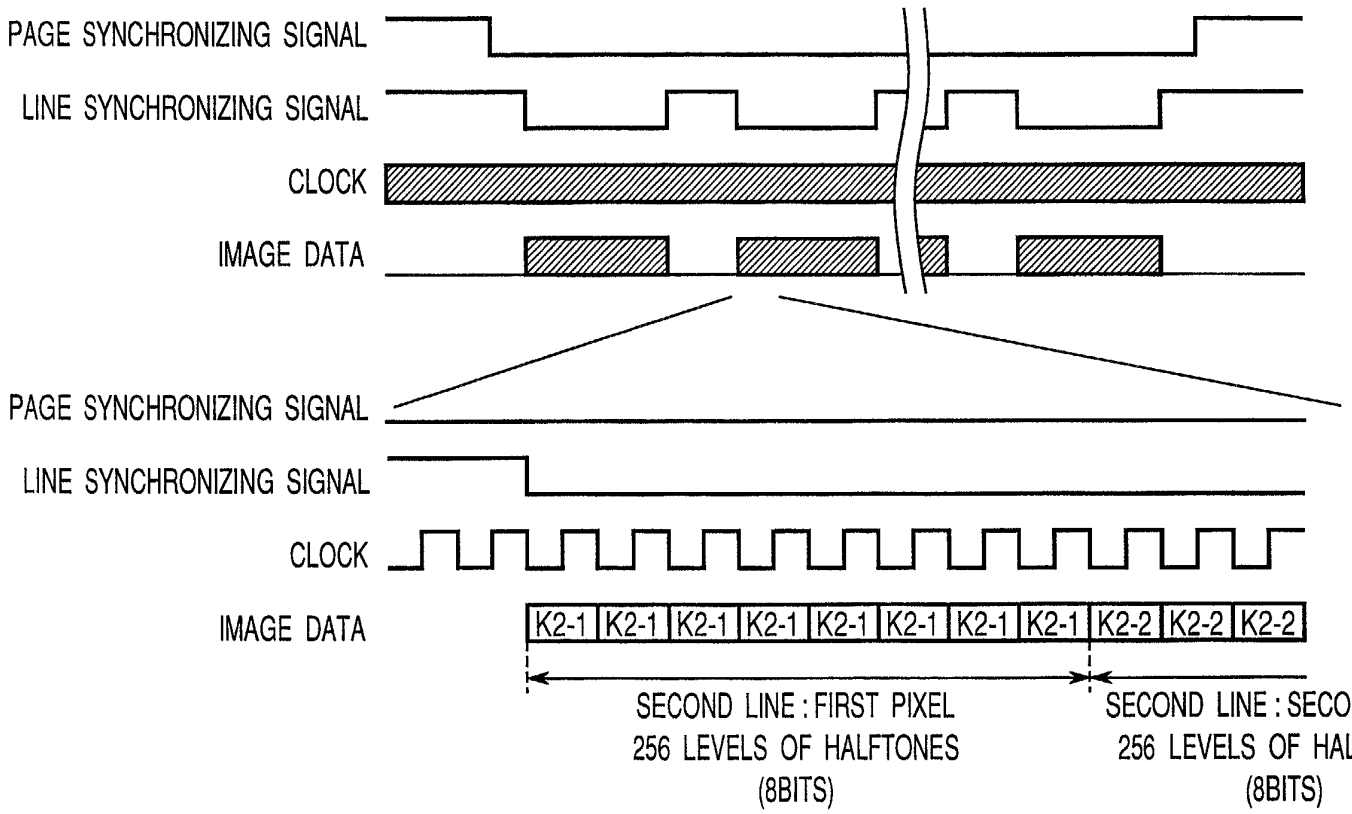

PAGE SYNCHRONIZING SIGNAL
LINE SYNCHRONIZING SIGNAL
CLOCK
IMAGE DATA
PAGE SYNCHRONIZING SIGNAL
LINE SYNCHRONIZING SIGNAL
CLOCK
IMAGE DATA
K2-1 K2-1 K2-1 K2-1 K2-1 K2-1 K2-1 K2-1 K2-2 K2-2 K2-2
SECOND LINE : FIRST PIXEL
256 LEVELS OF HALFTONES
(8BITS)
SECOND LINE : SECOND PIXEL
256 LEVELS OF HALFTONES
(8BITS)

Fig.5A

Fig.5B

Fig.6

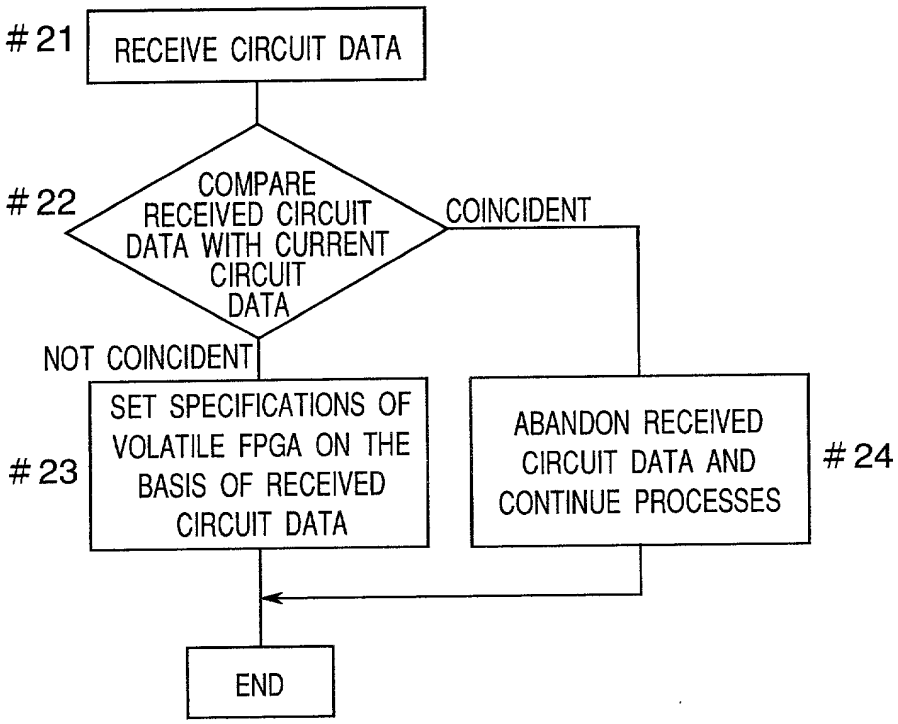

#21
RECEIVE CIRCUIT DATA
#22
COMPARE RECEIVED CIRCUIT DATA WITH CURRENT CIRCUIT DATA
COINCIDENT
NOT COINCIDENT
#23
SET SPECIFICATIONS OF VOLATILE FPGA ON THE BASIS OF RECEIVED CIRCUIT DATA
ABANDON RECEIVED CIRCUIT DATA AND CONTINUE PROCESSES
#24
END

Fig.7

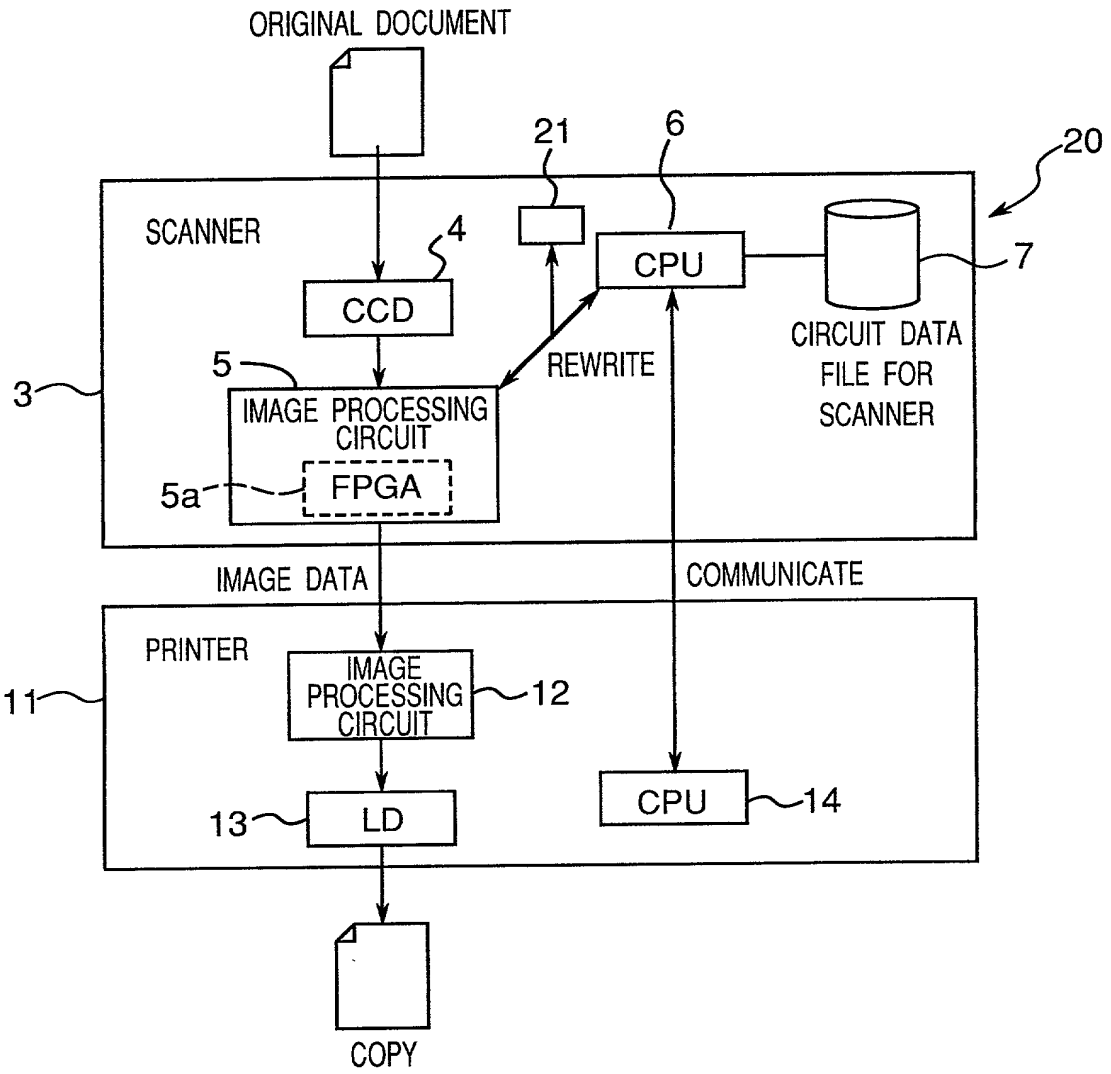

ORIGINAL DOCUMENT
21
6
20
SCANNER
4
CPU
7
CCD
CIRCUIT DATA
FILE FOR
SCANNER
5
REWRITE
3
IMAGE PROCESSING
CIRCUIT
5a
FPGA
IMAGE DATA
COMMUNICATE
PRINTER
IMAGE
PROCESSING
CIRCUIT
12
11
CPU
14
13
LD
COPY

Fig.8

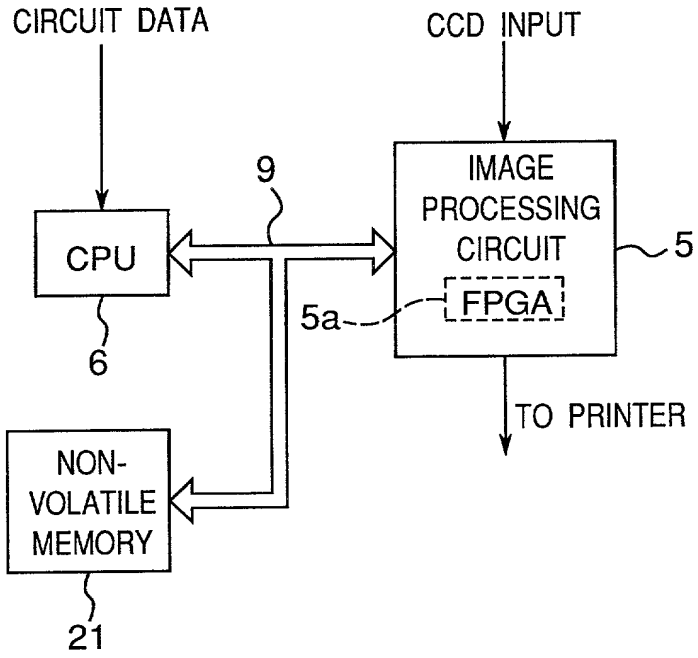

CIRCUIT DATA
CCD INPUT
9
IMAGE PROCESSING CIRCUIT
5
CPU
FPGA
5a
6
TO PRINTER
NON-VOLATILE MEMORY
21

Fig.9A

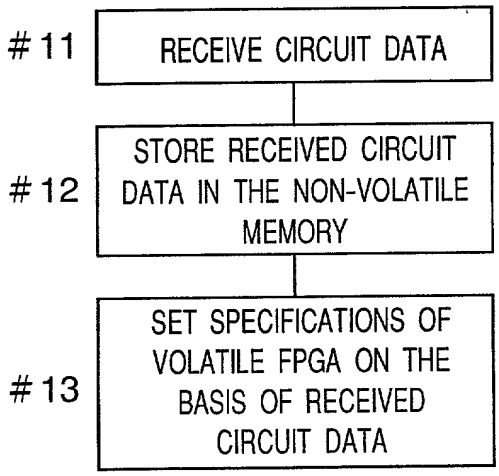

#11
RECEIVE CIRCUIT DATA
#12
STORE RECEIVED CIRCUIT DATA IN THE NON-VOLATILE MEMORY
#13
SET SPECIFICATIONS OF VOLATILE FPGA ON THE BASIS OF RECEIVED CIRCUIT DATA

Fig.9B

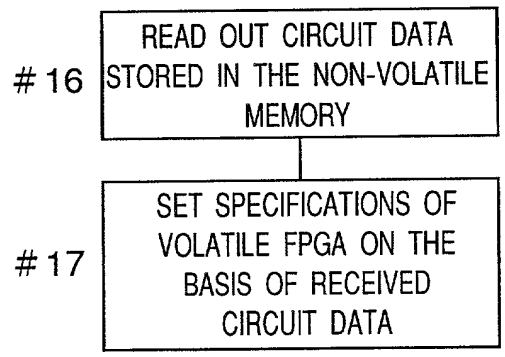

#16
READ OUT CIRCUIT DATA STORED IN THE NON-VOLATILE MEMORY
#17
SET SPECIFICATIONS OF VOLATILE FPGA ON THE BASIS OF RECEIVED CIRCUIT DATA

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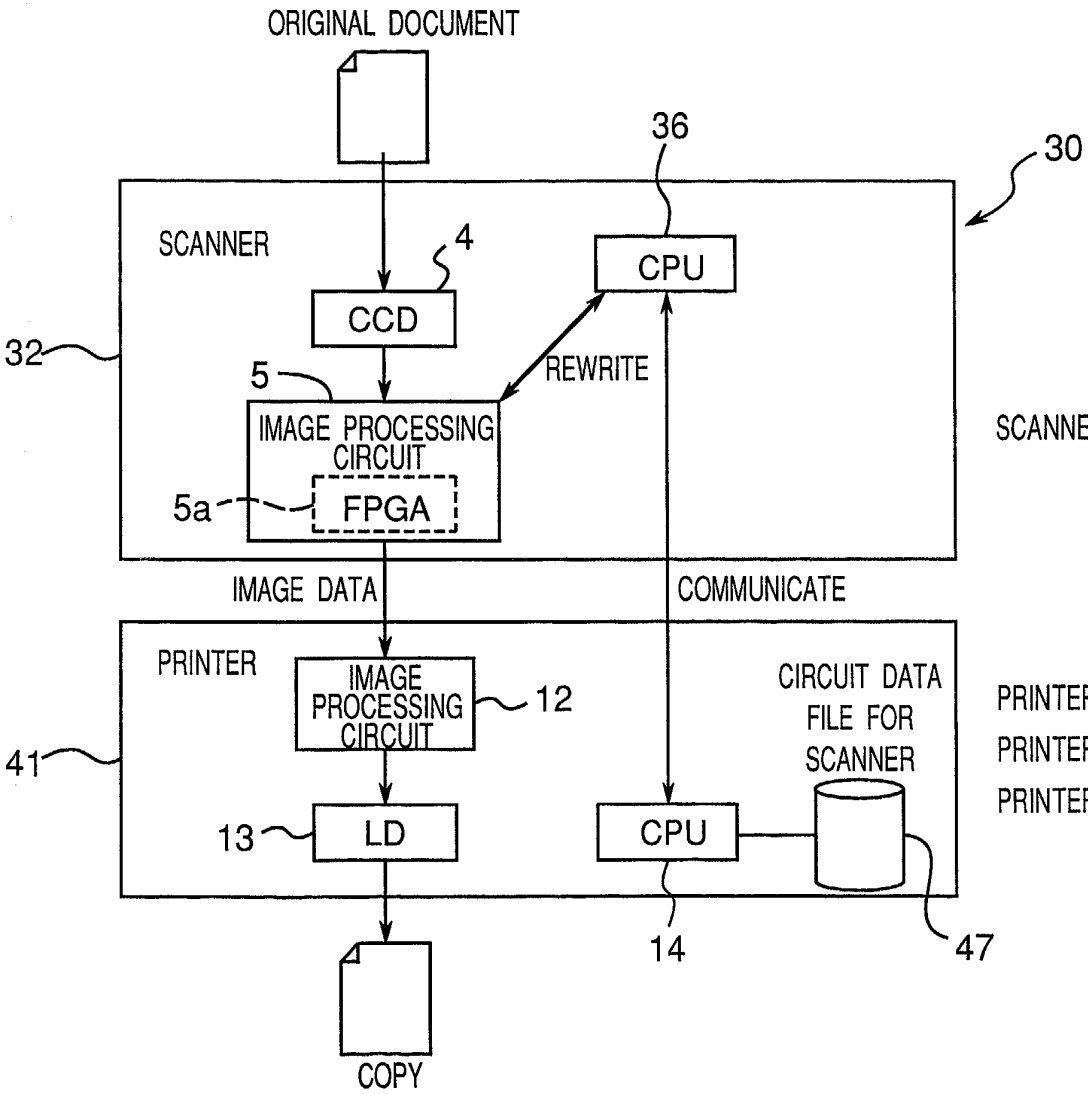
Fig.10



SCANNER=600dpi, COLORED, 256 LEVELS OF HALFTONES

PRINTER A : 600dpi, COLORED, 256 LEVELS OF HALFTONES
PRINTER B : 1,200dpi, MONOCHROME, 2 LEVELS OF HALFTONES
PRINTER C : 600dpi, MONOCHROME, 256 LEVELS OF HALFTONES

Fig.11

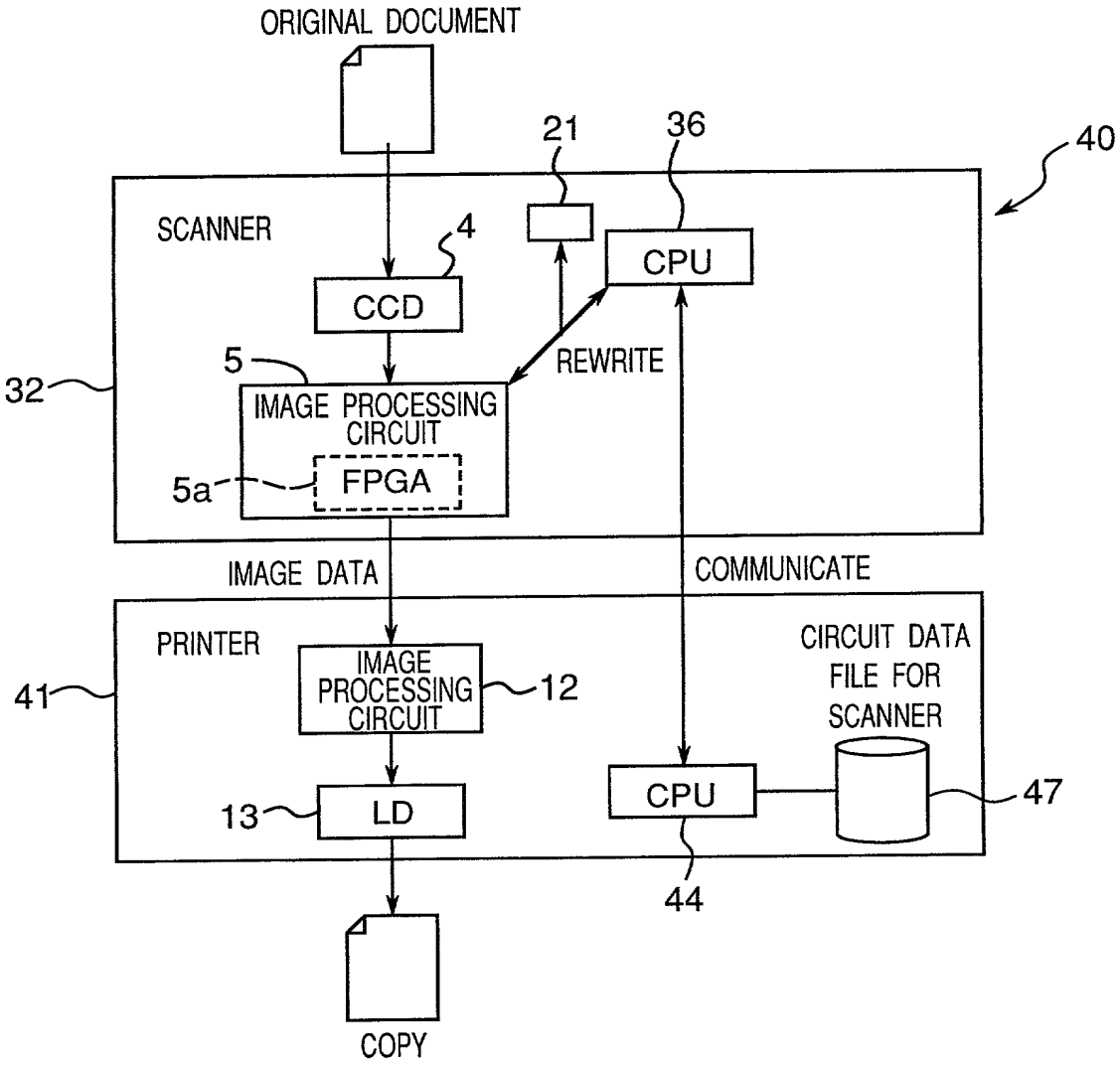

ORIGINAL DOCUMENT
21
36
40
SCANNER
4
CPU
CCD
5
REWRITE
32
IMAGE PROCESSING CIRCUIT
5a
FPGA
IMAGE DATA
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
12
CIRCUIT DATA FILE FOR SCANNER
41
13
LD
CPU
47
44
COPY

Fig.12

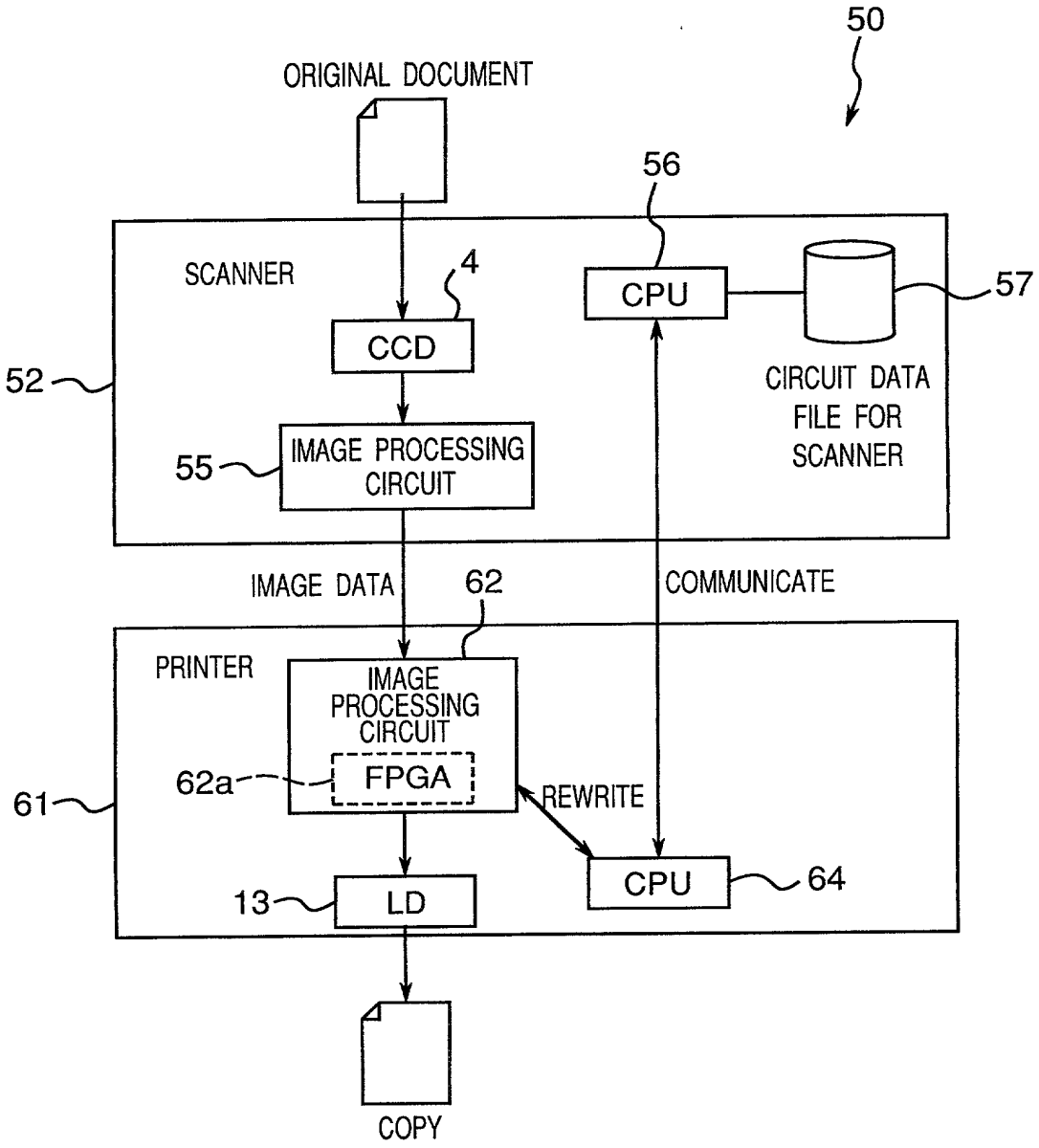

50
ORIGINAL DOCUMENT
56
SCANNER
4
CPU
57
CCD
52
CIRCUIT DATA FILE FOR SCANNER
55
IMAGE PROCESSING CIRCUIT
IMAGE DATA
62
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
62a
FPGA
61
REWRITE
CPU
64
13
LD
COPY

Fig.13

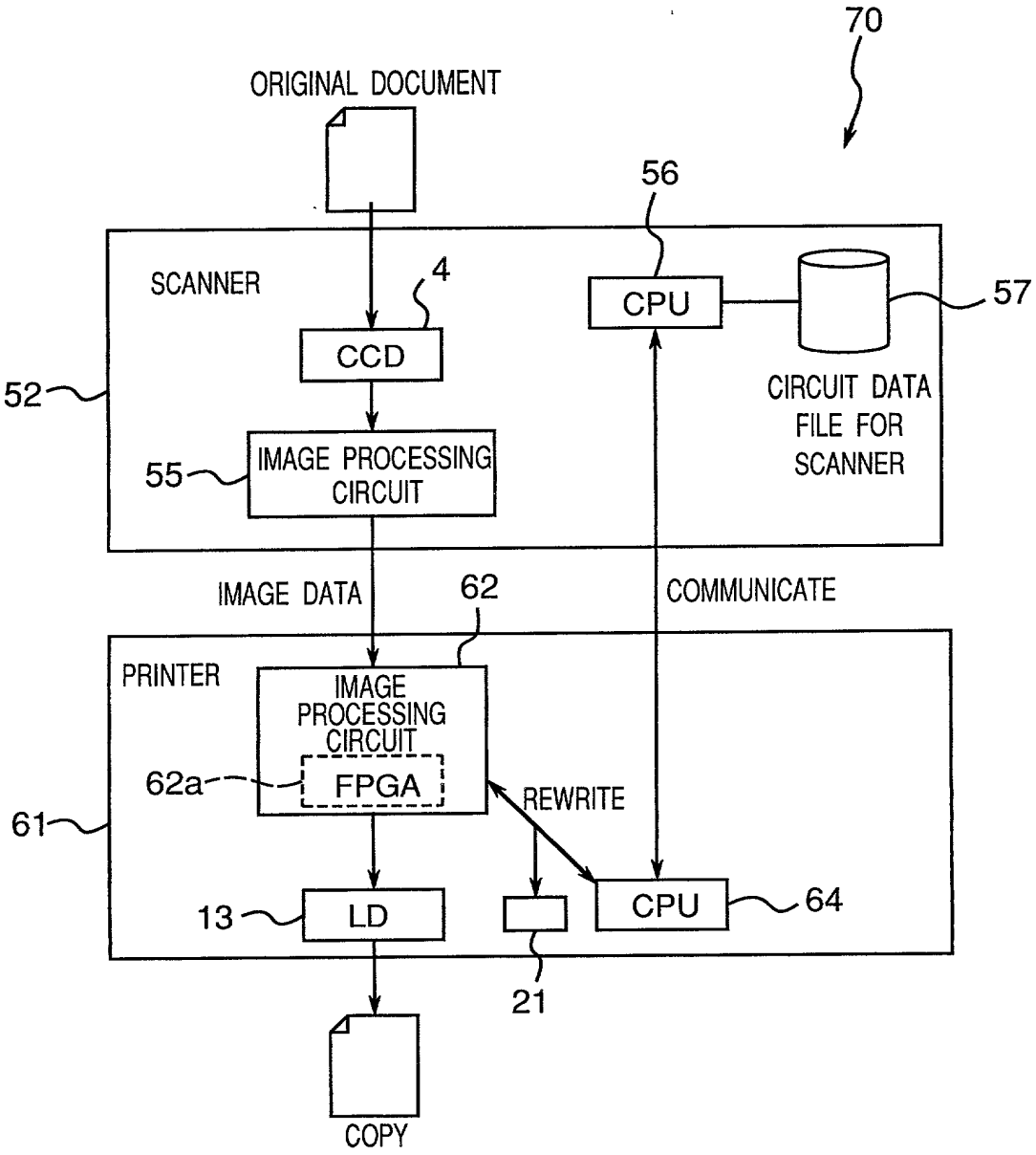

70
ORIGINAL DOCUMENT
56
SCANNER
4
CPU
57
CCD
52
CIRCUIT DATA FILE FOR SCANNER
55
IMAGE PROCESSING CIRCUIT
IMAGE DATA
62
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
62a
FPGA
REWRITE
61
13
LD
CPU
64
21
COPY

Fig.14

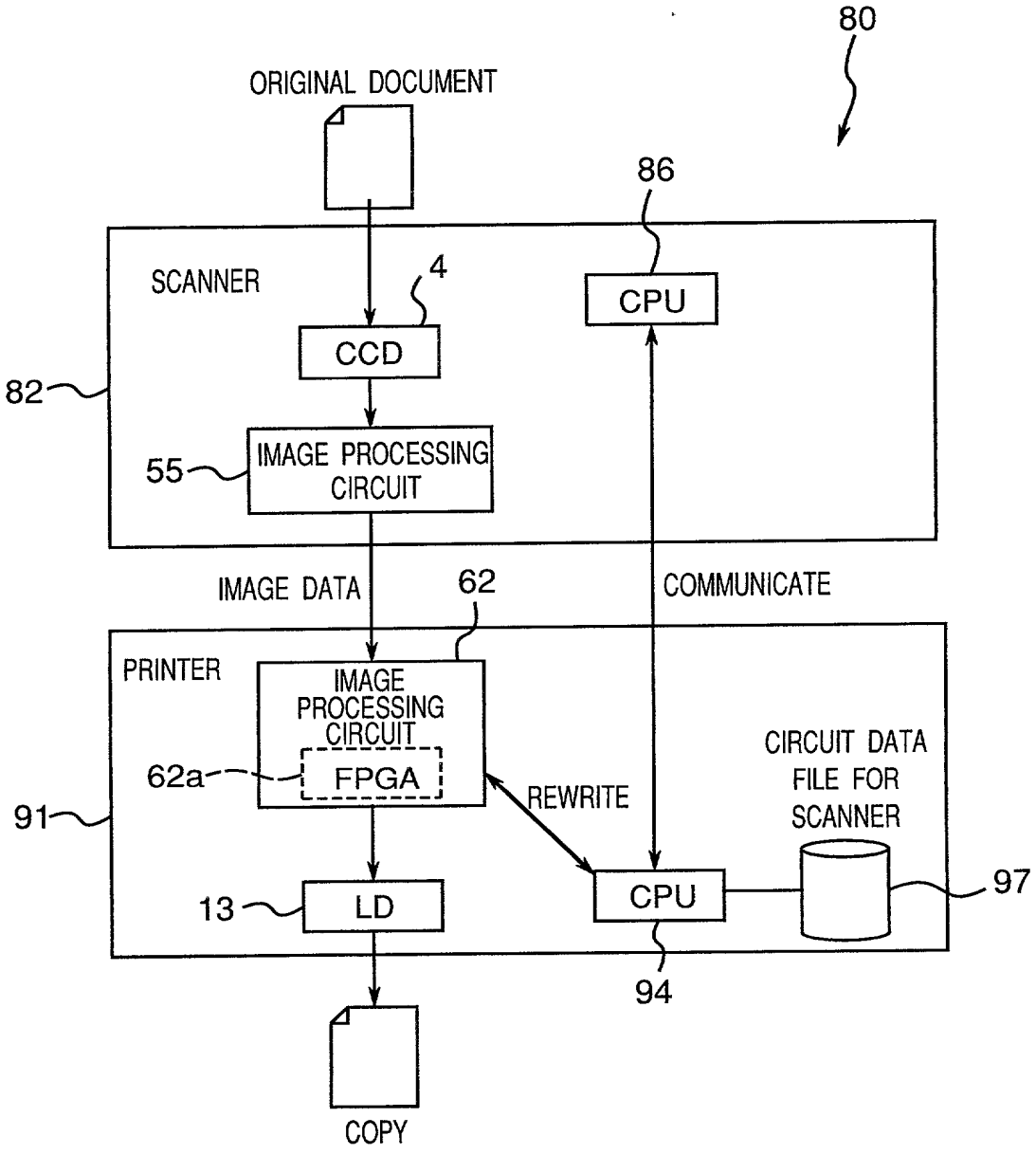

80
ORIGINAL DOCUMENT
86
SCANNER
4
CPU
CCD
82
IMAGE PROCESSING CIRCUIT
55
IMAGE DATA
62
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
CIRCUIT DATA FILE FOR SCANNER
62a
FPGA
REWRITE
91
13
LD
CPU
97
94
COPY

Fig.15

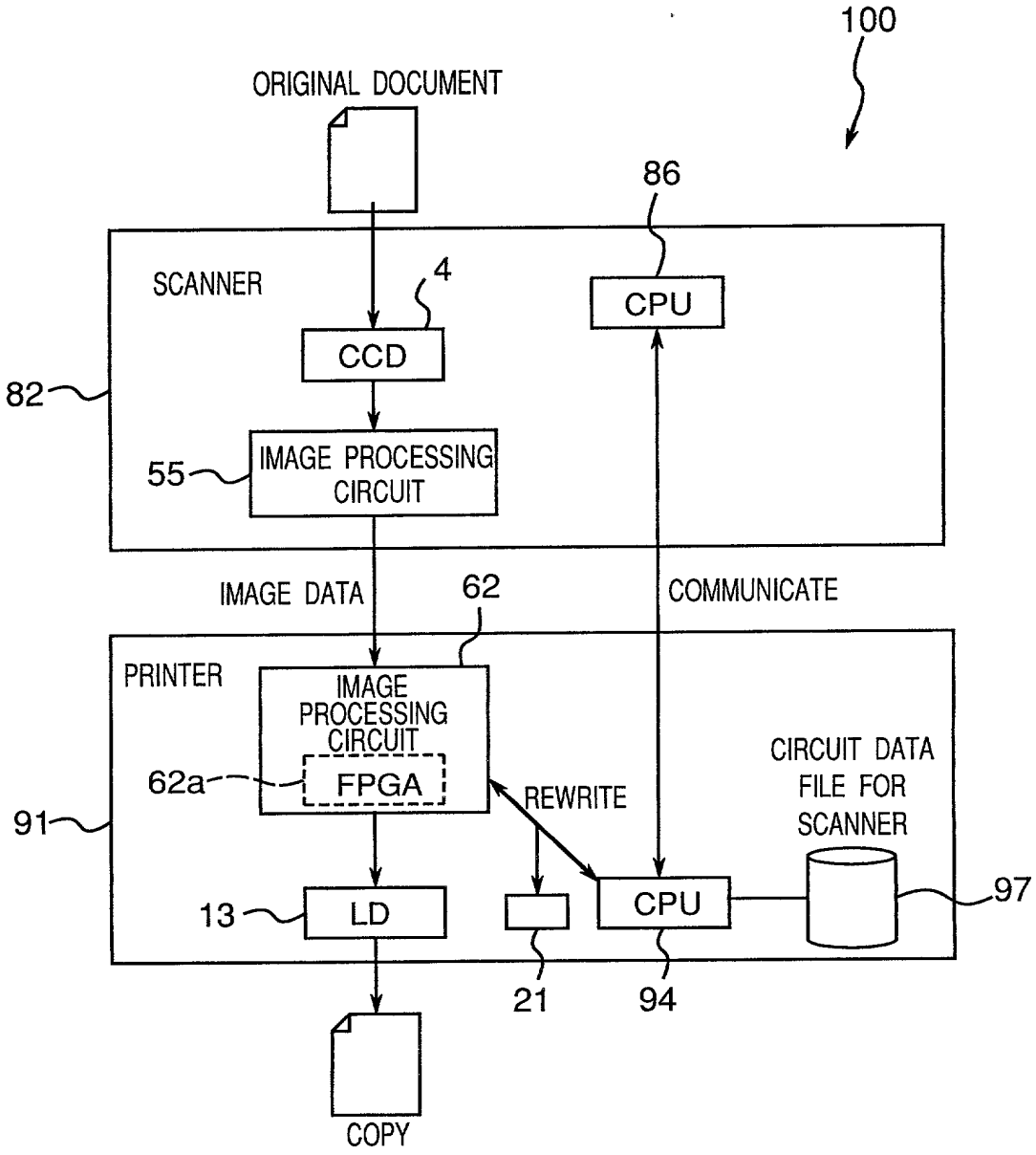

100
ORIGINAL DOCUMENT
86
SCANNER
4
CPU
CCD
82
IMAGE PROCESSING CIRCUIT
55
IMAGE DATA
62
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
62a
FPGA
REWRITE
CIRCUIT DATA FILE FOR SCANNER
91
13
LD
CPU
97
21
94
COPY

Fig.16

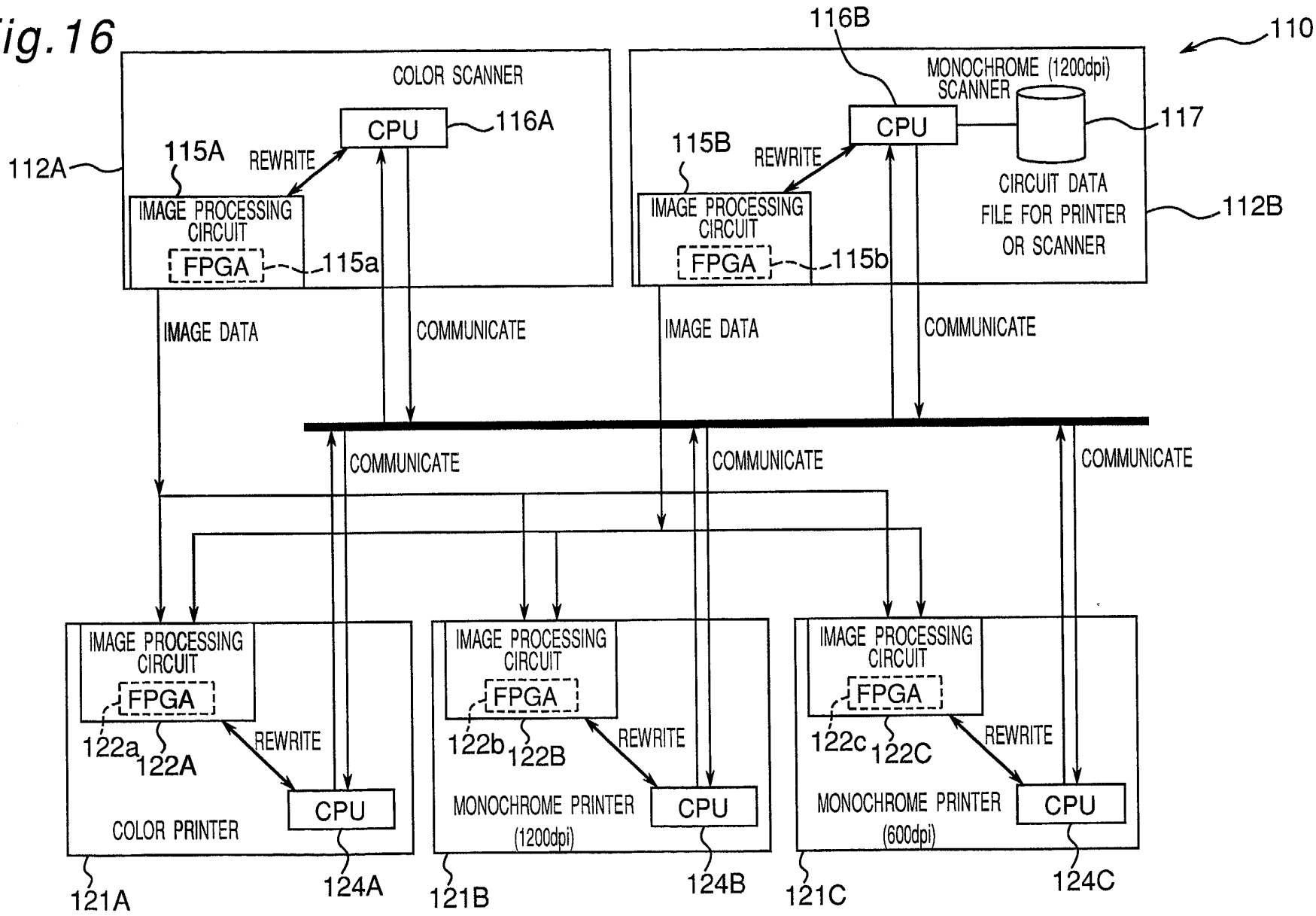

110
116B
COLOR SCANNER
CPU
116A
112A
115A
REWRITE
IMAGE PROCESSING CIRCUIT
FPGA
115a
MONOCHROME (1200dpi) SCANNER
117
115B
CIRCUIT DATA FILE FOR PRINTER OR SCANNER
112B
115b
IMAGE DATA
COMMUNICATE
122a
122A
122b
122B
122c
122C
COLOR PRINTER
MONOCHROME PRINTER
(1200dpi)
(600dpi)
121A
124A
121B
124B
121C
124C

Fig.17A

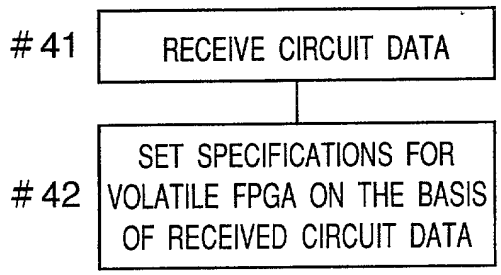


Fig.17B

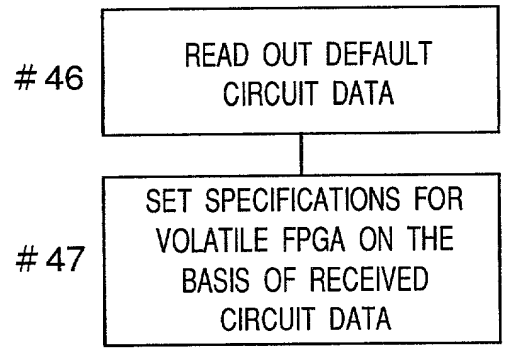


Fig. 18

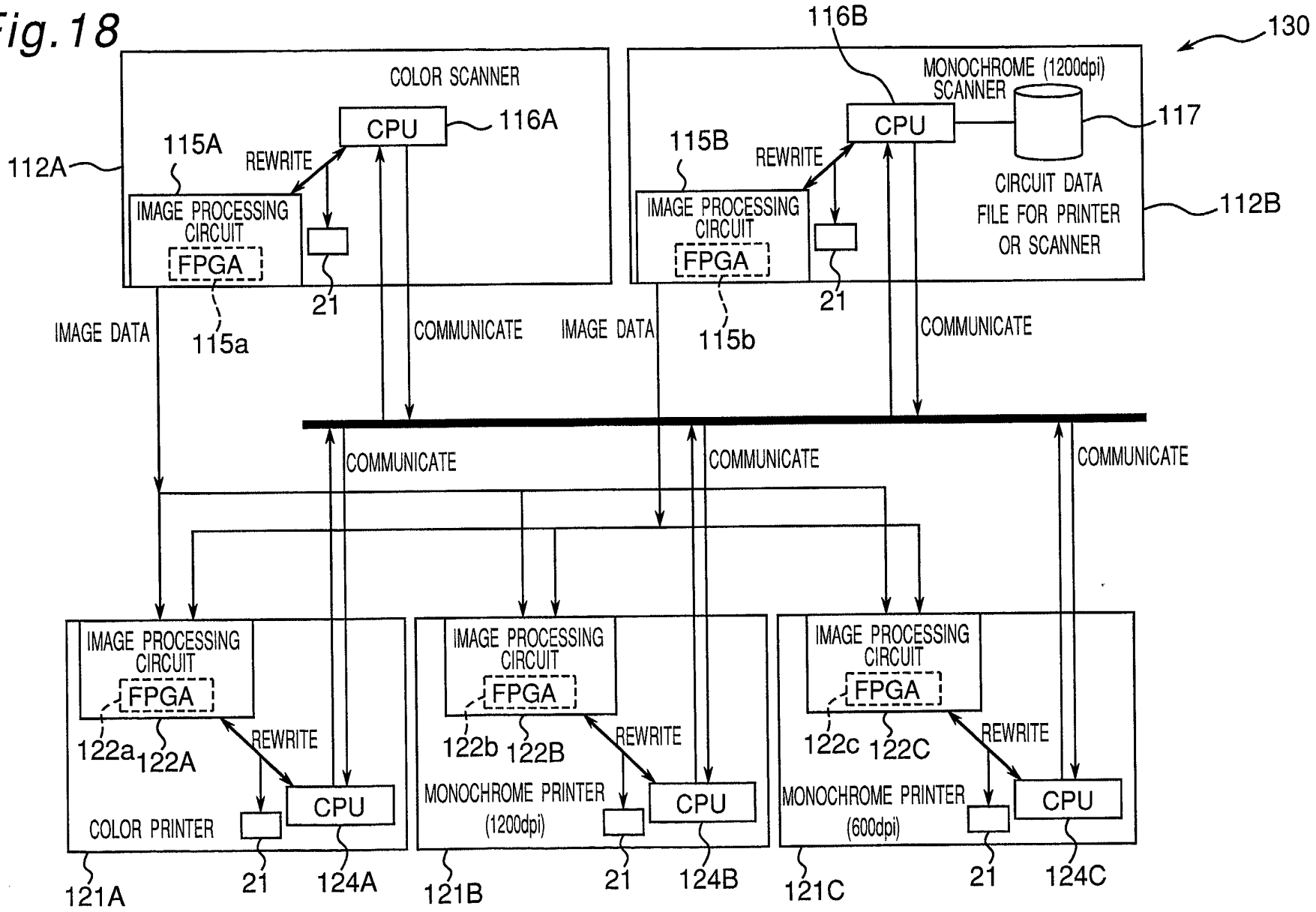
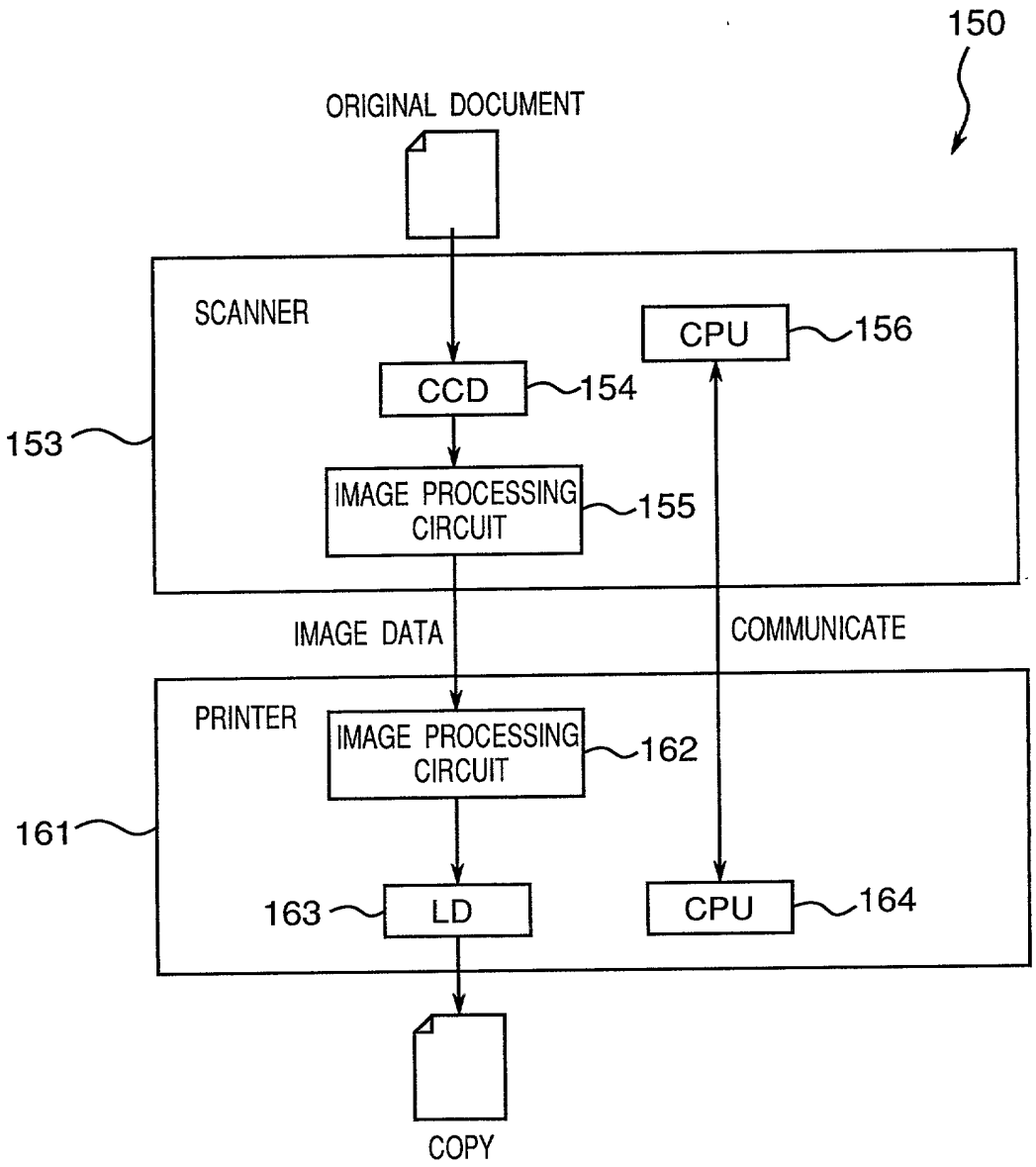

130
116B
COLOR SCANNER
CPU
116A
115A
REWRITE
112A
IMAGE PROCESSING CIRCUIT
FPGA
21
MONOCHROME (1200dpi) SCANNER
CPU
117
115B
REWRITE
CIRCUIT DATA FILE FOR PRINTER OR SCANNER
112B
IMAGE PROCESSING CIRCUIT
FPGA
21
IMAGE DATA
115a
COMMUNICATE
IMAGE DATA
115b
COMMUNICATE
COMMUNICATE
COMMUNICATE
COMMUNICATE
IMAGE PROCESSING CIRCUIT
FPGA
122a
122A
REWRITE
CPU
COLOR PRINTER
21
124A
121A
IMAGE PROCESSING CIRCUIT
FPGA
122b
122B
REWRITE
MONOCHROME PRINTER (1200dpi)
CPU
21
124B
121B
IMAGE PROCESSING CIRCUIT
FPGA
122c
122C
REWRITE
MONOCHROME PRINTER (600dpi)
CPU
21
124C
121C

Fig.19


150
ORIGINAL DOCUMENT
SCANNER
CPU
156
CCD
154
153
IMAGE PROCESSING CIRCUIT
155
IMAGE DATA
COMMUNICATE
PRINTER
IMAGE PROCESSING CIRCUIT
162
161
163
LD
CPU
164
COPY